memory integrated circuit] during periods of data access activity, [said] a variable voltage supplied at said first level being less than a variable voltage supplied at said second level, [during said periods of no data access activity than during said periods of data access activity, whereby power consumption of said memory integrated circuit is curtailed] wherein the power supplied at the first level is greater than or equal to a power necessary to preserve information stored in the integrated memory circuit and the power supplied at the second level is greater than or equal to the power required to read and write information in the integrated memory circuit.

21. (Twice Amended) An integrated circuit for controlling [the] a level of power supplied to a solid state memory integrated circuit having a first operation period for maintaining information stored in said memory integrated circuit, a second operation period for refreshing data stored in said memory integrated circuit, and a third operation period for accessing said memory integrated circuit, said memory integrated circuit having a first voltage requirement during said first operational period, a second voltage requirement during said second operational period and a third voltage requirement during said third operational period, said integrated circuit comprising:

power control means for supplying a variable voltage to said memory integrated circuit; and

logic control means for causing said power control means to supply to said memory integrated circuit a first voltage during said first operation period, a second voltage different from said first voltage during said second operation period, and a third voltage different from said first and second voltages during said third operation period.

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23. (Thrice amended) A dynamic power management device for supplying power to a solid state memory integrated circuit in a computer system having a power source supplying a substantially constant voltage, said dynamic power management device comprising:

power control means coupled to said power source for supplying a variable voltage to said memory integrated circuit, said variable voltage being less than or equal to said substantially constant voltage supplied by said power source; and

logic control means for generating address and control signals for said memory integrated circuit and for controlling said power control means;

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wherein the power control means [to] supply power to said memory integrated circuit, said power being supplied to the memory integrated circuit at a first level [to maintain memory information in said memory integrated circuit] during periods of no data access activity[,] and [to supply power] at a second level [to read and write memory information in said memory integrated circuit] during periods of data access activity, [said] a variable voltage supplied at said first level being less than a variable voltage supplied at said second level, [during said periods of no data access activity than during said periods of data access activity, whereby power consumption of said memory integrated circuit is curtailed]

wherein the power supplied at the first level is greater than or equal to a power necessary to preserve information stored in the integrated memory circuit and the power supplied at the second level is greater than or equal to the power required to read and write information in the integrated memory circuit.

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